

Atmel AVR211: Wafer Level Chip Scale Packages

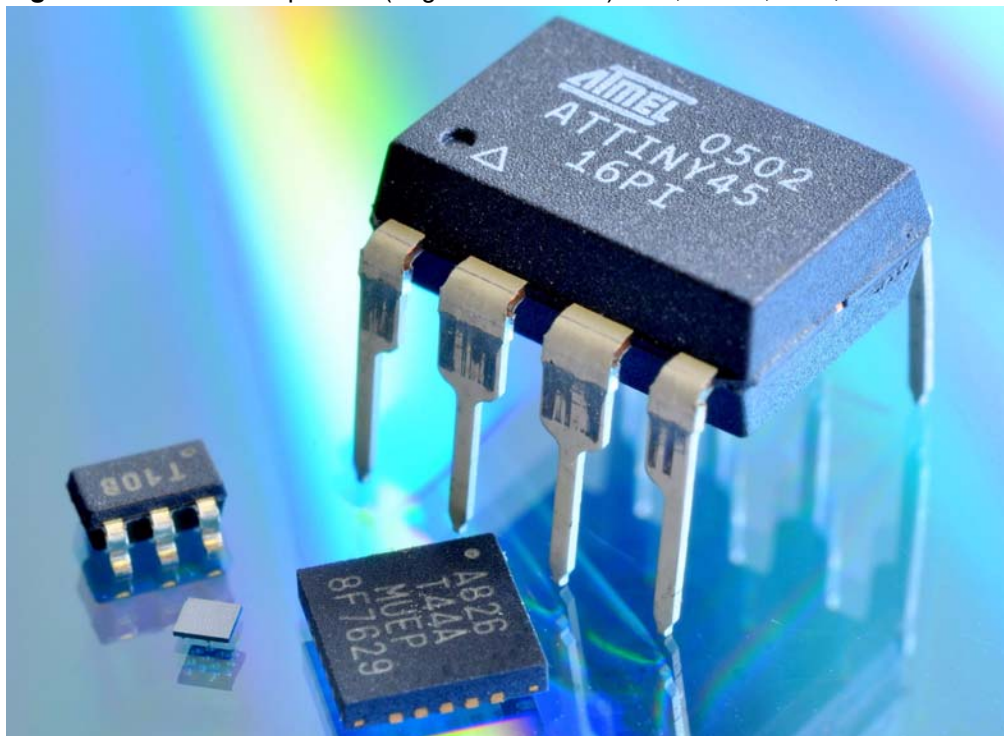
Features

- Allows integration using the smallest possible form factor
 - Packaged devices are practically the same size as the die
- Small footprint and package height
- Low inductance between die and PCB
- High thermal conduction characteristics
- Short manufacturing cycle time
- Light-weight: no leadframe, mold compound or substrate

1. Introduction

Wafer Level Chip Scale Packaging (WLCSP) refers to the technology of packaging an integrated circuit at wafer level, resulting in a device practically the same size as the die. While the name implies devices would be packaged the bare die is actually modified to add environmental protection layers and solder balls that are then used as the direct connection to the package carrier or substrate. WLCSP technology allow devices to be integrated in the design using the smallest possible form factor. WLCSP devices require no additional process steps on surface mount assembly lines.

Figure 1-1. Size comparison (largest to smallest): DIP, VQFN, SOT, and WLCSP.



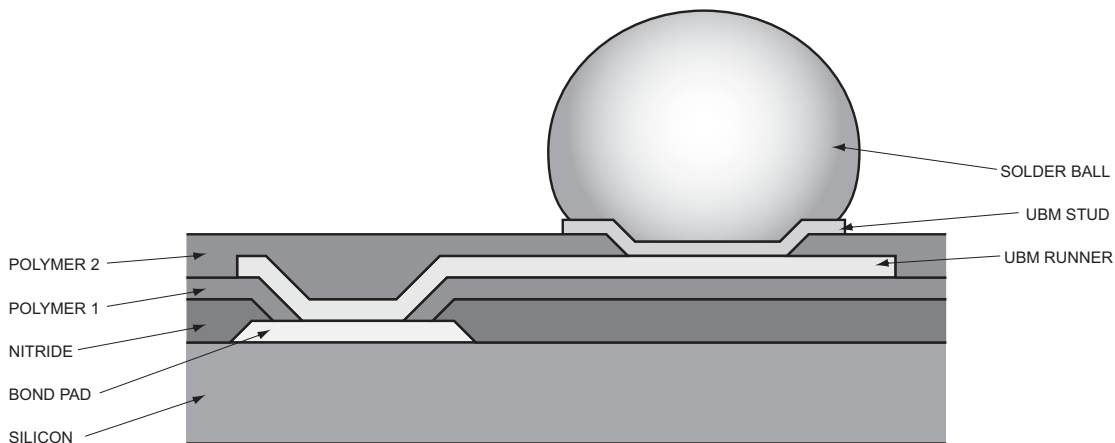
8-bit Atmel Microcontrollers

Application Note

2. Overview

The traditional process of packaging integrated circuits includes sawing the devices from the silicon wafer, attaching the devices onto a leadframe or substrate carrier, wirebonding the devices to the leadframe or substrate and then overmolding to form the final packages. In Wafer Level Chip Scale Packaging, the bare die is processed to have solder balls attached directly to the device, removing the need for external casing and wiring. See [Figure 2-1](#).

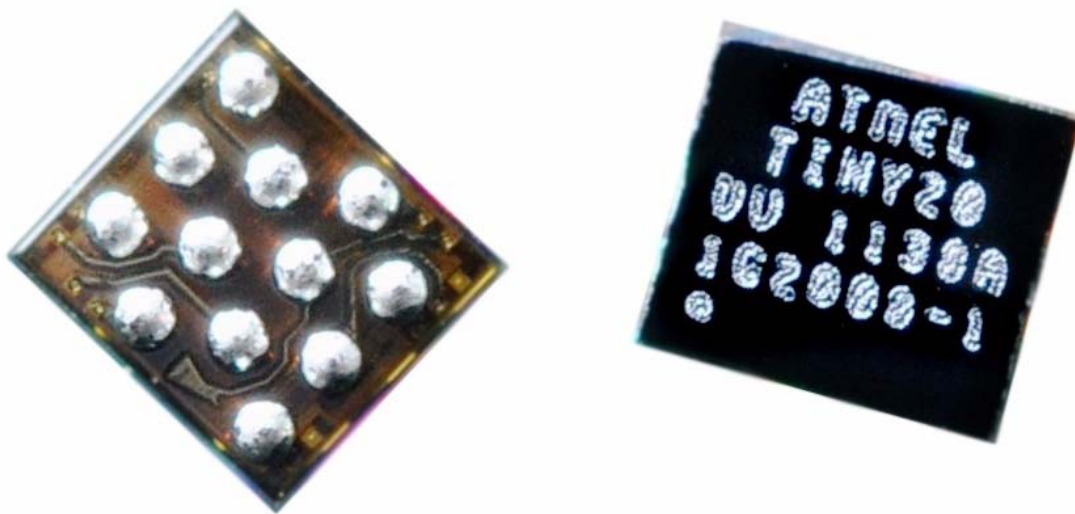
Figure 2-1. Cross section of part of the Atmel® WLCSP device.



The silicon die is covered with a nitride passivation layer, except for pad openings. A polymer dielectric is then added, followed by a metallic compound re-distribution trace layer. Another polymer dielectric layer is added, followed by the Under Bump Metallization (UBM) deposition. A solder ball is attached onto each UBM stud.

After processing, the device is essentially a die with an array pattern of solder balls, attached at a pitch compatible with traditional circuit board assembly processes. There is no need for external packaging material to protect the chip. See [Figure 2-2](#).

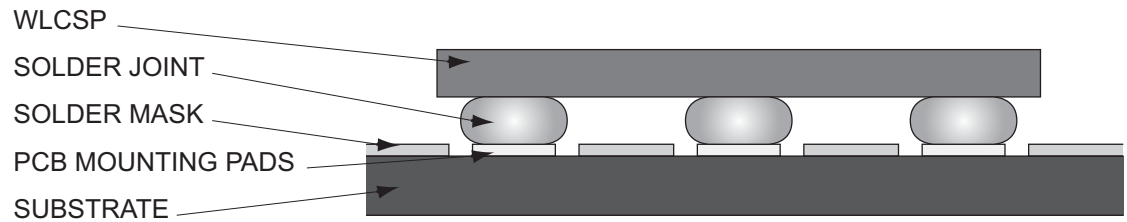
Figure 2-2. Atmel ATtiny20 WLCSP, bottom and top view.



2.1 Mounting

Dies are placed bump side down on the substrate metal lands and the electrical connection is then made using a reflow process to melt the solder and form the joint. See [Figure 2-3](#).

Figure 2-3. Atmel WLCSP device mounted on PCB.



The solder attaches the die to the substrate. Optionally, an electrically-insulating underfill is added to further enhance the reliability of the solder joint.

3. Printed circuit board design

Typically, use of WLCSP requires advanced PCB manufacturing methods, high accuracy pick-and-place machinery and special QA inspection tools.

Some general guidelines for PCB design are listed in [Table 3-1](#).

Table 3-1. General recommendations for PCB design.

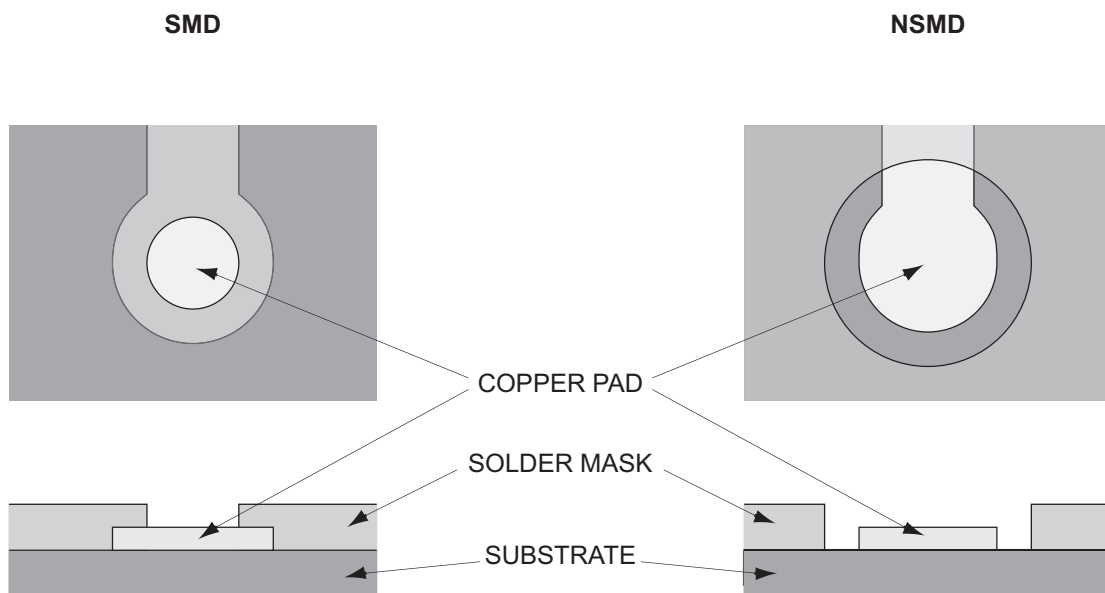
Parameter	Condition	Recommended
Copper thickness		30µm
Copper finish		OSP (Organic Solderability Preservative)
Solder mask thickness		≤ 25.4µm
Pad shape		Round
Pad diameter	SMD	No max. limit (depend on routing spacing)
	NSMD	0.225 ... 0.250µm ⁽¹⁾
Trace width	SMD	< ½ pad diameter
	NSMD	≤ 100µm

Note: 1. Atmel ATtiny20 device.

3.1 Land patterns

There are two methods for constructing pad land patterns; Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD). In SMD, the opening of the solder mask on the board is smaller than the underlying copper area. In NSMD, the land pattern has a solder mask opening larger than the copper pad. See [Figure 3-1](#).

Figure 3-1. Solder mask defined and non-solder mask defined land patterns.



Either pad construction method can be used with WLCSP.

A comparison of SMD and NSMD land patterns is shown in [Table 3-2](#).

Table 3-2. SMD vs. NSMD land patterns.

Parameter	Solder mask defined	Non-solder mask defined
Copper land area	Large	Small
	Good adhesion of land to board	Uniform surface finish
Solder form	Narrow solder joint	Solder flow around land
Solder size	High stand-off	Low stand-off
Solder bond	High stress concentration	Low stress concentration
Fatigue life	Medium	Long

The recommended construction method is NSMD.

3.2 Via-in-pad

Although PCB trace routing issues may be resolved by the use of via-in-pads, structures like this are not recommended. This is because via-in-pads can cause critical voids in the interface of solder joints.

If via-in-pads must be used, it is recommended to use filled vias.

3.3 Solder stencil

Solder paste is typically applied to lands using a stencil. Solder print stencils can be fabricated using a process of chemical etch, laser cut, or electroforming. The recommended method is laser cut with electropolish, as this gives a good quality to cost ratio.

See [Table 3-3](#) for recommended stencil options.

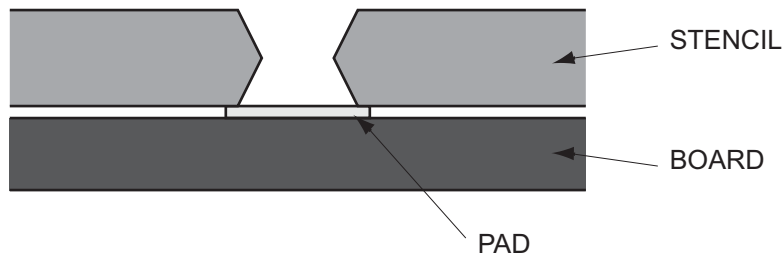
Table 3-3. Recommended stencil options.

Parameter	Value	Unit
Pitch	0.400	mm
Pad footprint (diameter)	0.250	mm
Aperture width	0.250	mm
Aperture length	0.250	mm
Stencil foil thickness	0.073 – 0.125	mm

3.3.1 Chemical etch

A resist is applied to the stencil material and apertures are defined photographically. Unexposed areas are then chemically etched away, resulting in apertures. Etching is carried out from both sides, leaving a waist within the apertures. See [Figure 3-2](#). Apertures can be smoothed by electropolishing.

Figure 3-2. Chemically etched aperture.

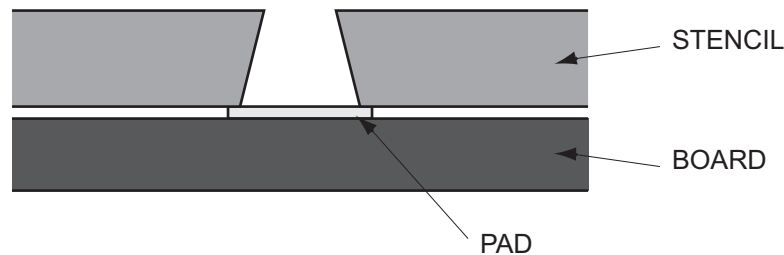


Chemically etched stencils have poor release characteristics, especially at smaller pitches, but are less expensive than stencils fabricated using other methods.

3.3.2 Laser cut

A laser is used to cut the perimeters of apertures, leaving rougher wall structures than other stencil fabrication methods. See [Figure 3-3](#). The rough wall structures caused by the melting effect of the laser beam can be adjusted by polishing or electroplating.

Figure 3-3. Laser cut aperture.



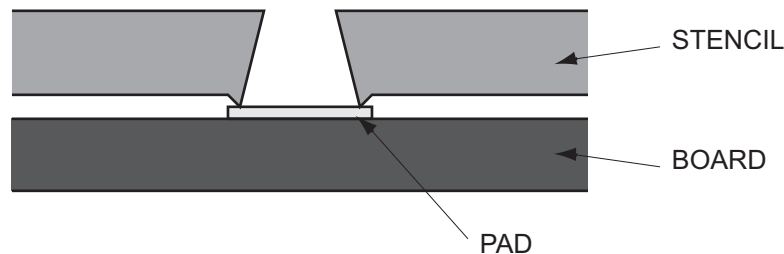
Laser cutting results in trapezoidal apertures with good release characteristics. This is a fabrication method with high accuracy, allowing finer stencil details.

Since this is a serial process where apertures are formed one at a time, the cost is typically higher than for example chemical etch, where the entire substrate is processed at the same time. But when finished off with electropolish laser cutting gives a good quality to cost ratio.

3.3.3 Electroformed

A resist is applied to the stencil material and aperture patterns are defined photographically. The stencil is then grown around the aperture patterns using electrolytic plating. This results in smooth, tapered aperture walls. See [Figure 3-4](#).

Figure 3-4. Electroformed aperture.



Electroformed stencils are expensive but have very good quality, wear and release characteristics.

3.4 Solder paste

A solder paste with SAC 405 alloy composition, 90% metal content and no-clean flux is recommended. Particle size Type 3 is suitable for printing with pitches down to 0.4mm (16mil), but Type 4 may be required with ultra fine pitch WLCSP.

3.5 Solder printing

It is recommended to use 3D Automatic Optical Inspection (AOI) for post verification of solder printing.

3.6 Pick & placement

Placement accuracy is a critical issue in surface mount technology. See [Table 3-4](#) for required accuracy.

Table 3-4. Required placement accuracy.

Pitch	Accuracy requirement	Unit
0.40mm	±0.03	mm

3.7 Reflow soldering

During reflow soldering the circuit board and the components that are held to it by solder paste are heated and cooled in a controlled manner, making the components stick to the board properly.

The reflow soldering steps are as follows:

1. Rapid temperature increase. This step evaporates the solvent from the paste and burns off the largest amount of contaminants.
2. Dwell at uniform temperature. This is to preheat the assembly, making sure all joints stabilise around the dwell temperature. Also, this step is important to ensure the solder is fully dried before entering reflow temperature.
3. Rapid temperature spike. This step makes the solder paste reflow and wets the surfaces of both component and board pads. Solder reflow starts happening when the paste is taken to a temperature above the melting point of the solder, but this temperature must be exceeded by some 20°C to ensure quality reflow.
4. Controlled cooling. The first stage (down to the liquidus temperature) is critical but solder continues to be mechanically weak at temperatures above 150°C, so care has to be taken to avoid rapid changes of temperature, draughts, etc. Allowing the components to cool in a well controlled manner can prevent thermal shock and ensure a successful reflow soldering process.

The recommended solder reflow profile is illustrated in [Figure 3-5](#) and [Table 3-5](#).

Figure 3-5. Solder reflow profile.

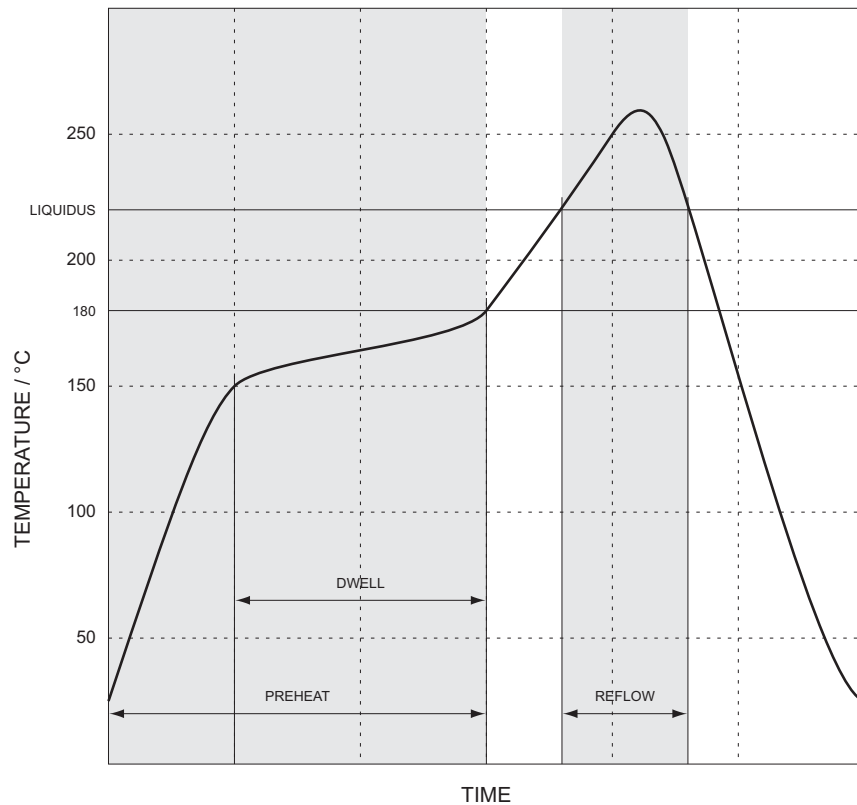


Table 3-5. Solder reflow parameters.

Process Step	Condition	Value
Ramp up rate	$T < 150^{\circ}\text{C}$	$< 3^{\circ}\text{C/s}$
Pre-heat time (including dwell time)	$T = 150 - 180^{\circ}\text{C}$	60 – 180s
Reflow time / Time Above Liquidus (TAL)	$T > 220^{\circ}\text{C}$	30 – 90s
Time at peak temperature	$T = 255 \pm 5^{\circ}\text{C}$	10 – 20s
Ramp down rate		$< 6^{\circ}\text{C/s}$

4. Printed circuit board rework

Sometimes, PCB rework may call for removal of a device. Once removed, a WLCSP device cannot be re-used and must be replaced.

Replacement WLCSP devices must be handled on the backside, using a vacuum pick-up tool, since tweezers can easily cause chipping damages at device edges.

The recommended PCB rework procedure is as follows:

1. Preheat the board to 150 – 170°C.
2. Apply direct heat to the WLCSP device: 240 – 250°C for up to 90 seconds.
3. Remove WLCSP device.
4. Redress site with soldering iron and solder wick or vacuum de-soldering.
5. Clean rework site.
6. Apply solder paste.
7. Use a vacuum wand to pick up new WLCSP at the backside. Place the device onto the solder pad site.
8. Apply local heat to reflow the solder for attachment.
9. Perform appropriate cleaning.

5. Reference

Table 3-5 below lists miscellaneous WLCSP related details.

Table 5-1. WLCSP miscellaneous details.

Parameter	Value
Die size	Depends on device
Number of balls	Depends on die size
Ball pitch	400µm ⁽¹⁾
Solder ball material	SAC405 ⁽²⁾

Notes: 1. 350µm on request.
2. SL35 on request.

5.1 Device drawings

For the most up to date WLCSP drawings, see device datasheets.

5.2 Carrier information

For the most up to date carrier drawings and information, see Atmel web pages.

5.3 Device availability

For the most up to date list of devices available in WLCSP, see Atmel web pages.

6. Revision history

6.1 Rev. 42007A – 06/12

Initial revision.

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